



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 53080
 Shiro SAKIYAMA, et al. : Confirmation Number: 6689
 Application No.: 10/511,165 : Group Art Unit: 2816
 Filed: October 14, 2004 : Examiner: HILTUNEN, THOMAS J
 :
 For: SEMICONDUCTOR INTEGRATED CIRCUIT WITH REDUCED SPEED VARIATIONS

REQUEST FOR CORRECTED FILING RECEIPT

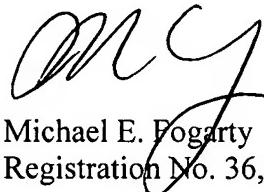
Mail Stop OFR
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Sir:

Attached is a copy of the Filing Receipt received from the U.S. Patent and Trademark Office in the above-referenced application. It is noted that **the number of claims listed on the official filing receipt is incorrect. Attached is a copy of the Preliminary Amendment, which evidences that the number of claims should now be: 2 independent claims and 9 dependent claims totaling 11 claims.** It is requested that a corrected filing receipt be issued.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Michael E. Fogarty
 Registration No. 36,139

600 13th Street, N.W.
 Washington, DC 20005-3096
 Phone: 202.756.8000 MEF:ksa
 Facsimile: 202.756.8087
 Date: October 1, 2007

Please recognize our Customer No. 53080
 as our correspondence address.



UNITED STATES PATENT AND TRADEMARK OFFICE

OCT 01 2007
U.S. PATENT & TRADEMARK OFFICE
OCT 01 2007
OCT 01 2007

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPL NO.	FILING OR 371(C) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	TOT CLMS	IND CLMS
10/511,165	10/14/2004	2816	1250	71971-015	16	3 11 2

CONFIRMATION NO. 6689

20277
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

CORRECTED FILING RECEIPT



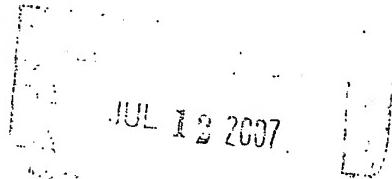
OC000000024721304

Date Mailed: 07/09/2007

Receipt is acknowledged of this nonprovisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Shiro Sakiyama, Yawata-shi, Kyoto, JAPAN;
Masayoshi Kinoshita, Settsu-shi, JAPAN;
Masaya Sumita, Amagasaki-shi, JAPAN;



Power of Attorney: The patent practitioners associated with Customer Number 20277

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP04/01942 02/19/2004

Foreign Applications

JAPAN 2003-047418 02/25/2003

If Required, Foreign Filing License Granted: 09/22/2006

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US10/511,165**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

Semiconductor integrated circuit with reduced speed variations

Preliminary Class

327

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER Title 35, United States Code, Section 184 Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-5. (Cancelled)

6. (Previously presented) A semiconductor integrated circuit, comprising:
a main circuit including a plurality of MOS transistors of a MOS structure in which a source potential and a substrate potential are separated from each other, and operating while receiving a predetermined operating power supply voltage; and
a substrate potential control circuit for controlling the substrate potential of a MOS transistor in the main circuit so that an actual saturation current value of the MOS transistor is equal to a target saturation current value that is sufficient to satisfy a desired operation speed of the main circuit given the operating power supply voltage value of the main circuit, the substrate potential control circuit, including:
a constant current generation circuit;
a current-voltage conversion circuit including a MOS transistor provided therein and having current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor provided therein for converting a constant current value of the constant current generation circuit to a voltage value; and

a differential amplifier circuit for controlling a substrate potential of the current-voltage conversion circuit so that the voltage value generated by the current-voltage conversion circuit is equal to the predetermined operating power supply voltage value of the main circuit,

wherein the substrate potential control circuit controls the substrate potential of each of the MOS transistors in the main circuit so that the substrate potential is equal to the substrate potential of the current-voltage conversion circuit controlled by the differential amplifier circuit.

7. (Original) The semiconductor integrated circuit of claim 6, wherein where the predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the constant current value of the constant current generation circuit is proportional to the operating power supply voltage value within the operating voltage range.

8. (Original) The semiconductor integrated circuit of claim 6, wherein where the predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the constant current value of the constant current generation circuit is in a linear function relationship with the operating power supply voltage value within the operating voltage range.

9. (Original) The semiconductor integrated circuit of claim 6, wherein:

the main circuit has a plurality of operating power supply voltage ranges;

the constant current value of the constant current generation circuit is in a linear function relationship with an operating power supply voltage value within an operating voltage range for each operating power supply voltage range of the main circuit; and

the linear function relationship between the constant current value of the constant current generation circuit and the operating power supply voltage value is different for each operating power supply voltage range.

10. (Original) The semiconductor integrated circuit of claim 6, wherein the constant current generation circuit generates a plurality of constant current values, and selectively outputs one of the plurality of constant current values.

11. (Original) The semiconductor integrated circuit of claim 6, wherein the constant current generation circuit generates a constant current with a variation rate smaller than that for the actual saturation current value of the MOS transistors of the main circuit.

12. (Original) The semiconductor integrated circuit of claim 11, wherein the constant current generation circuit includes an adjustment circuit for reducing variations in the generated constant current value.

13. (Previously presented) A semiconductor integrated circuit, comprising:
a main circuit including a plurality of MOS transistors of a MOS structure, and operating while receiving an operating power supply voltage; and

a power supply voltage control circuit for controlling the operating power supply voltage supplied to the main circuit, wherein:

a target saturation current value of the MOS transistors that is sufficient to satisfy a desired operation speed of the main circuit given a predetermined power supply voltage, is set in the power supply voltage control circuit; and

the power supply voltage control circuit controls a voltage value of the operating power supply voltage supplied to the main circuit so that an actual saturation current value of the MOS transistors in the main circuit is equal to the target saturation current value.

14. (Original) The semiconductor integrated circuit of claim 13, wherein the target saturation current value of the MOS transistors of the main circuit is a target saturation current value of an nMOS transistor or that of a pMOS transistor from among the MOS transistors of the main circuit, or is an average value between the target saturation current values of the nMOS and pMOS transistors.

15. (Previously Presented) The semiconductor integrated circuit of claim 13, wherein the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with the operating power supply voltage supplied to the main circuit.

16. (Previously Presented) The semiconductor integrated circuit of claim 13, wherein:
- the main circuit includes a plurality of operating power supply voltage ranges;
 - the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with an operating power supply voltage value within an operating voltage range for each operating power supply voltage range of the main circuit;
 - the linear function relationship between the target saturation current value and the operating power supply voltage value is different for each operating power supply voltage range.